Techniques for Stabilizing Power Operational Amplifiers

1.0 INTRODUCTION

It is unlikely that a power op amp would always be employed to drive a purely resistive load. For if that were the case, stability would never become a problem. On the other hand, a load which is largely capacitive does present stability issues as will become clear in this Application Note. In a pure capacitor, the voltage lags the charging current by 90 degrees, so there is a large phase delay in the loop response of a feedback circuit. Such a phase delay can be a significant contributor to instability.

Let's get started by considering any multistage amplifier. It will begin to exhibit a roll off in open loop gain (A_{OL}), as well as an increase in phase delay at higher frequencies because of the low-pass filters that are formed by nodes with finite source impedances driving capacitive loads within the amplifier stage[1]. So a load that is largely capacitive, together with the capacitance within a multistage amplifier, can bring about instability since the phase lag may be approaching, and perhaps exceed 180 degrees. It is this phase delay that is a key contributor to instability. When instability occurs, it can transform a power amplifier into an oscillator, inadvertently, and the device is likely to become quite hot and fail in as little as one second.

In the discussion that follows, there are some simple techniques for managing phase and gain relationships to maintain a stable circuit.

1.1 LOOP STABILITY VERSUS NON-LOOP STABILITY

In this Application Note we discuss Loop Stability. Whereas 'Non-Loop Stability' that denotes issues such as layout, power-supply bypassing and proper grounding are discussed in Reference 2. In this Application Note we will examine:

- Why capacitive loads create stability problems in standard op amp circuits.
- Closed loop gain (1/ß) and open loop gain (A_{OL}) and their relationships to stability.
- How capacitors impact the open loop gain (A_{OL}) curve
- Three ways to adjust the closed loop gain (1ß) and the open loop gain (A_{OL}) responses to regain phase margin and stability, along with the advantages and disadvantages of each technique.

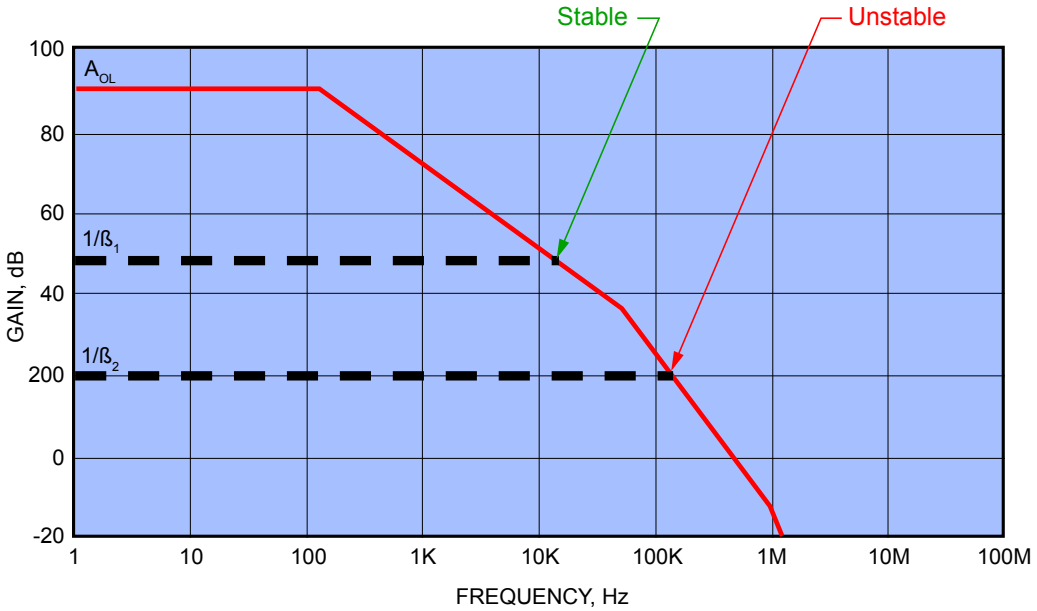


Figure 1. Stable or Unstable? − As we explain in this Application Note, modifying the closed loop gain (1/ß) is one of several effective ways of achieving stable operation.

Bode Plots in a nutshell

A Bode Plot of a power amplifier open loop gain (A_{OL}) response is usually a graph of the log of the magnitude plotted as a function of the log of the frequency, as depicted below. The magnitude axis is usually expressed in decibels. This transforms multiplication into a matter of simply adding vertical distances on the plot.

With this examination of the multistage amplifier, as discussed in Section 1.0, the open loop gain (A_{OL}) response is comparable to a single-pole low pass filter, as depicted in Figure 1.

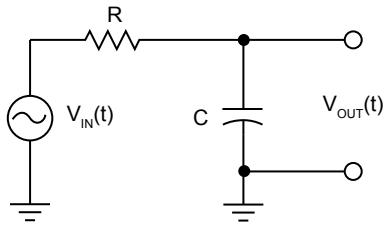
The Bode Plot of amplitude can be approximated by straight lines, as shown at the lower right. Note that as the straight-line approximation approaches the corner frequency the true value, shown by the dotted line, departs from the straight-line approximation and is actually 3.01 dB below the junction of the two intersecting straight line segments.

Note that for corner frequencies much lower than 1, the approximation is a straight line which covers the portion where the capacitive reactance is large. For frequencies much larger than the corner frequency the curve is approximated by the straight line descending at rate of 20 dB per decade. This is due to the diminishing capacitance reactance at higher frequencies.

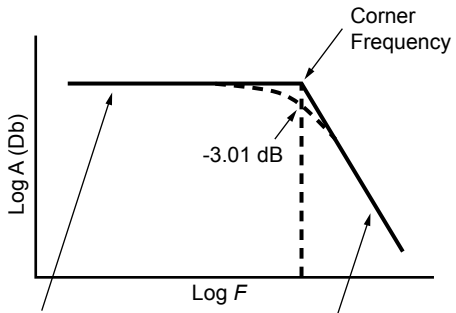
One could also prepare a Bode Plot for the log of the phase relationship between the input and output, but this is dispensed with for the analysis employed in this Application Note.

Op amps often exhibit more than one pole in their open loop gain (A_{OL}) Bode Plots.

Note that at the first corner frequency or pole there is a 90-degree phase shift. If there is a second pole the phase shift becomes 180 degrees above that frequency.



A Bode Plot



$$V_{OUT}(t) = \frac{\frac{1}{j2\pi fC}}{\frac{1}{j2\pi fC} + R} V_{IN}(t)$$

$$V_{OUT}(t) = \frac{1}{(1 + j2\pi fRC)} V_{IN}(t)$$

$$f = \frac{1}{2\pi RC} \triangleq \text{“Corner Frequency or Pole”}$$

2.0 EVOLUTION OF AN OPERATIONAL AMPLIFIER

Reviewing the evolution of an op amp is useful because it aids the understanding of the stability techniques. This example begins with an open loop amplifier (A_{OL}), with a gain as depicted in Figure 2(a).
So the open loop gain is simply:

$$V_{OUT} = A_{OL}\, V_{IN} \qquad (1)$$

Then add a summing point at the input as shown in Figure 2(b).

To convert the open loop amplifier into an operational amplifier we feed back a portion of the output which is ß $_{OUT}$, as shown in Figure 2(c). Then label the inputs and outputs so that the equation for V_{OUT} can be written by inspection:

$$V_{OUT} = A_{OL}(V_{IN} - ßV_{OUT}) \qquad (2)$$

or:

$$V_{OUT}(1 + A_{OL}ß) = A_{OL}V_{IN}$$

so that the closed loop gain A_{CL} is :

$$A_{CL} = \frac{V_{OUT}}{V_{IN}} = \frac{A_{OL}}{1 + A_{OL}ß} \qquad (3)$$

Because A_{OL} is large compared with 1 therefore A_{OL}ß will also be large compared with 1. Then the denominator 1 + A_{OL}ß is equal, approximately, to A_{OL}ß and equation (3) becomes simply:

$$A_{CL} \approx 1/ß \equiv \text{Closed loop gain} \qquad (4)$$

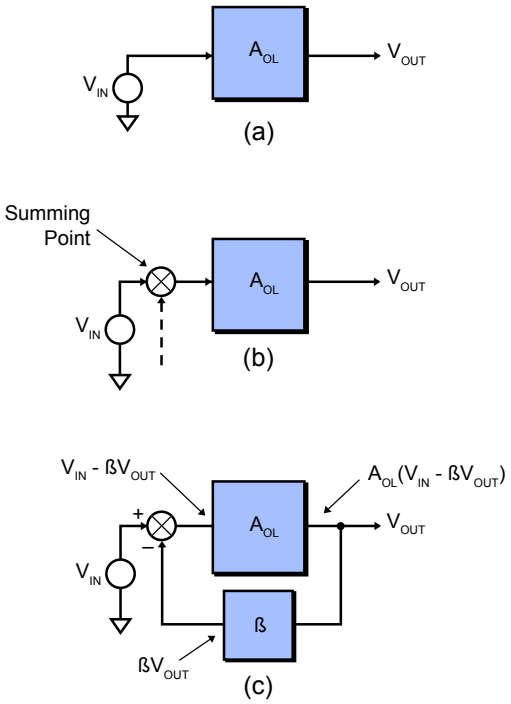


Figure 2. Evolution of an Op Amp

Key relationships . . .

A_{OL}	=	Open Loop Gain
1/ß	=	Closed Loop Gain
A_{OL} − 1/ß	=	Loop Gain − the signal propagating around the loop and available to reduce errors and non-linearities.

2.1 A CLOSER LOOK AT ß

Beta (ß) is the fraction of the output that is fed back to the input. In Figure 3(a) it is thereby given as:

$$V_{FB} = \frac{R_1}{R_1 + R_F} V_{OUT} \qquad (5)$$

$$V_{FB} = ß\ V_{OUT} \qquad (6)$$

Where: $ß = \frac{R_1}{R_1 + R_F}$

Or the non-inverting closed loop gain 1/ß is:

$$\frac{1}{ß} = \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1} \qquad (7)$$

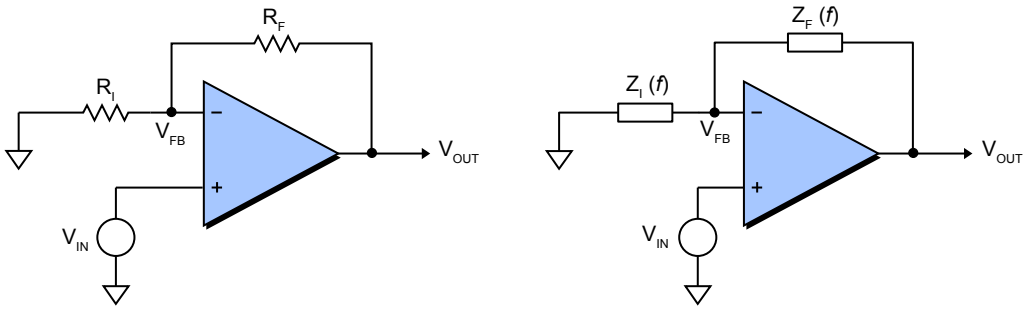
(Keep in mind that the current flowing into the two inputs is virtually zero.) If ß comprises solely resistors R_I and R_F then the closed loop gain (1/ß) line will plot as a horizontal straight line on a bode plot.

This is depicted in Figure 1 in which the $1/ß_1$ and $1/ß_2$ lines, which are the closed loop small signal gains, are depicted as a constant and frequency independent.

However, if Z_I and Z_F are capacitors or inductors − or some combination of capacitors, inductors and resistors − then Z_I and Z_F are functions of frequency:

$$V_{FB} = \frac{Z_I(f)}{Z_I(f) + Z_F(f)} V_{OUT} \qquad (8)$$

This means the Closed loop gain (1/ß) line does not plot as a straight line on a bode plot.



(a) (b)

Figure 3. Beta – Frequency Independent (a) and Frequency Dependent (b)

2.2 HOW AN OP AMP BEHAVES AS THE SIGNAL FREQUENCY RISES

This section depicts the fact that if there is a critical frequency (F_{CL}) at which the loop gain (A_{OL} - 1/ß) becomes zero, then the operational amplifier simply degenerates into an open loop amplifier with an open loop gain of A_{OL}. If that occurs the amplifier no longer behaves as an operational amplifier and its benefits simply vanish.

This is depicted in Figure 4 in which the closed loop (1/ß) line is a constant – which means the components of ß are independent of the frequency – or purely resistive. Note how the 1/ß value subtracts from the open loop gain (A_{OL}) at low frequencie. But once the A_{OL} line reaches the frequency F_{CL}, the loop gain (A_{OL} - 1/ß) becomes zero. So for frequencies above F_{CL}, the op amp becomes an open loop amplifier with a gain of A_{OL}.

Is the power amplifier unstable? That depends on the phase relationship between the input and output for the amplifier for frequencies of F_{CL} and above, as discussed in Section 2.3 that follows.

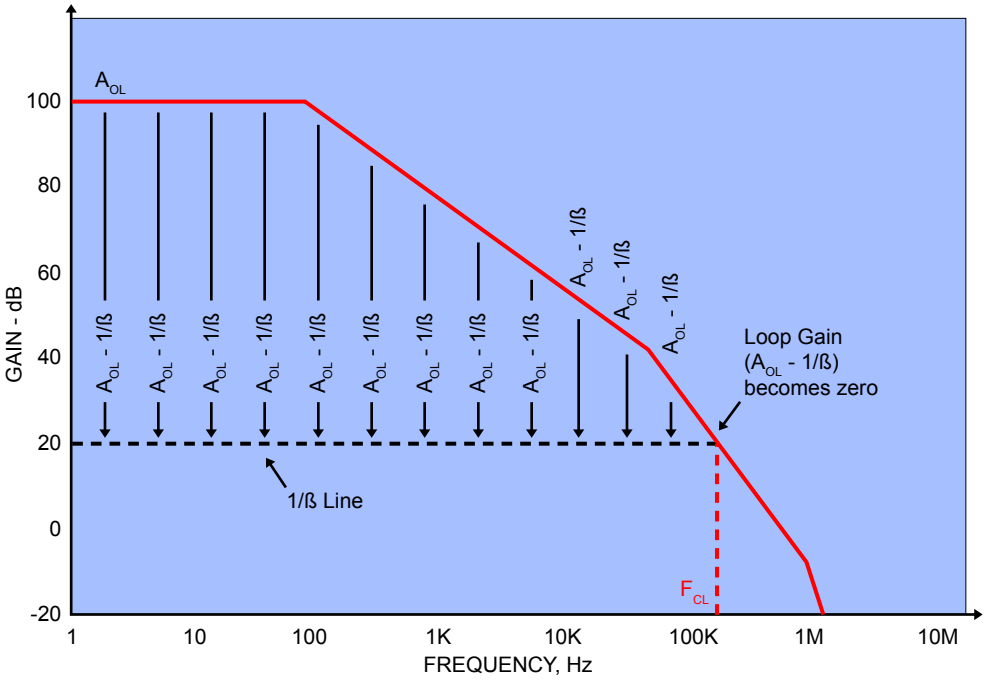


Figure 4. Closed Loop Constant – When the Loop Gain runs out of gas

2.3 PHASE MARGIN

Oscillation can occur if at a phase shift of 180 degrees the loop gain (1/ß) is one (0dB), or more. Consequently, the 'Phase Margin' is defined as how close the phase shift is to a full 180 degrees when the loop gain is 0dB, also called "The Point Of Intersection". A good rule of thumb is to design for 135 degrees of phase shift which constitutes a phase margin of 45 degrees. This will allow for events that occur during power up and power down – as well as other transient conditions which may cause changes in the open loop gain (A_{OL}) curve that could initiate transient oscillations.

Note that it is the included angle formed at the Point Of Intersection (closed loop gain = 0dB) which denotes stability (20dB/decade) or instability (40dB/decade, or more).

2.4 USABLE BANDWIDTH

The usable bandwidth is usually defined as the frequency at which the closed loop gain (A_{OL}-1/ß) falls to 20dB. The reason is that above this frequency the error rises above 10% so that the performance of the op amp is degraded significantly.

2.5 A FIRST ORDER CHECK FOR STABILITY

As we have explained, the loop gain (1/ß) is the amount of signal available for feedback to reduce errors and non-linearities. A first-order check for stability is to make sure that when the closed loop gain (1/ß) reaches the open loop gain (A_{OL}) line the phase shift is less than 180 degrees.

Shown in Figure 5 is a plot of an open loop gain A_{OL} which displays a descent rate of 20dB per decade at frequencies of approximately 100Hz to 80kHz. This denotes a phase shift of 90 degrees. At approximately 80kHz the descent rate changes to 40dB per decade. So above this frequency, the phase shift is 180 degrees.

Note that for a loop gain ($1/ß_1$) the plot intersects the open loop gain (A_{OL}) plot where its descent rate is 20 dB per decade. So this curve passes the first check for stability.

For a complete analysis we will need to check the phase shift of the open loop gain (A_{OL}) response over frequency. This is discussed in Section 4.

Note that the loop gain ($1/ß_2$) plot intersects the open loop gain (A_{OL}) plot where its rate of intersection is 40dB per decade. So this curve fails the first check for stability.

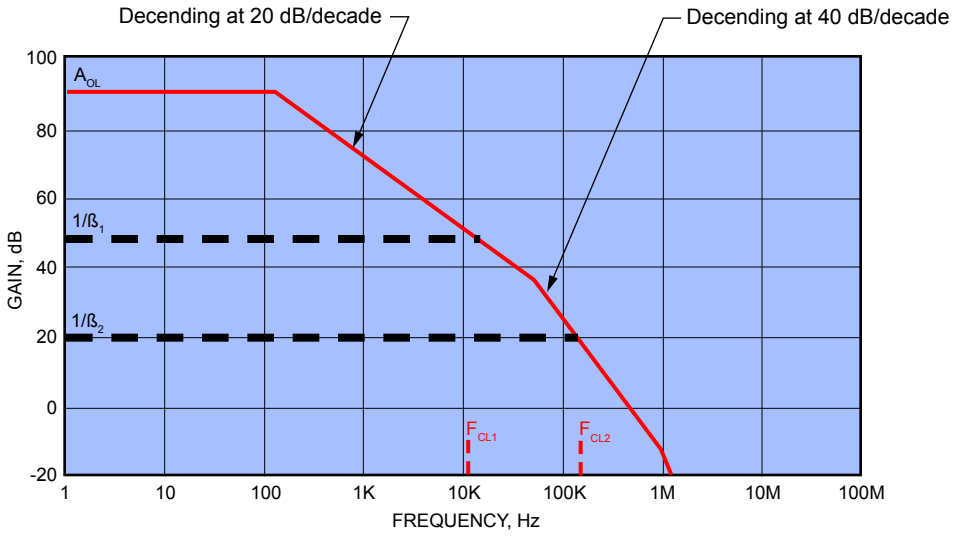


Figure 5. Stability Check – A first order check of stability

3.0 FOUR COMPENSATING TECHNIQUES – PHASE COMPENSATION

In most treatments of stability, phase compensation will never come up because most small signal amplifiers are internally compensated and therefore there is nothing that can be done externally to modify the amplifier. However, in almost every Apex amplifier the phase compensation can be controlled by an external capacitance C_C that the user can select. This enables moving the first pole of the open loop gain (A_{OL}) plot left or right in frequency, as depicted in Figure 6. By raising the value of C_C, the open loop gain (A_{OL}) plot can be moved to the left and down so that what would otherwise be a problem pole − a descent at 40dB per decade − moves below 0dB. Therefore it is no longer a problem with regard to stability.

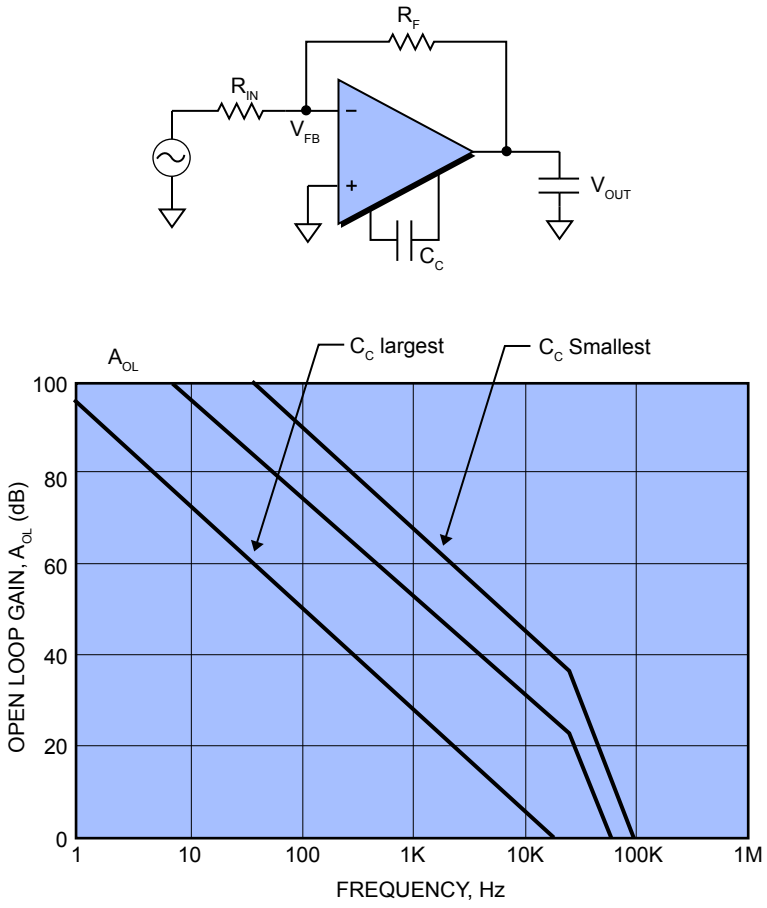


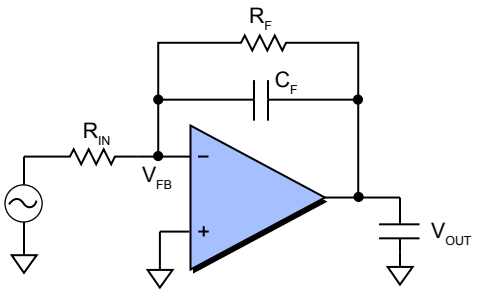
Figure 6. Phase Compensation

3.1 FEEDBACK ZERO COMPENSATION

As depicted in Figure 7, feedback zero compensation is a method of tailoring the op amp's performance for a given application. The goal is to alter the loop gain (1/ß) by adding a feedback capacitor C_F, placing a pole in the 1/ß plot so that it intersects the open loop gain (A_{OL}) line at 20db per decade instead of at 40dB per decade. The included angle of the intersection is now 20dB/decade. Hence it is stable. The usable bandwidth is approximately 10kHz.

This technique is very sensitive to the tolerances of the feedback because the loop gain (1/ß) plot is governed by the RC response of the feedback. Therefore the power amplifier is very susceptible to going in and out of stability based on capacitor C_F, which may change in value with changes in temperature

To summarize, this compensation technique is easy to implement when the loop gain (1/ß) value is large. But the technique is somewhat sensitive to variations in component tolerances.



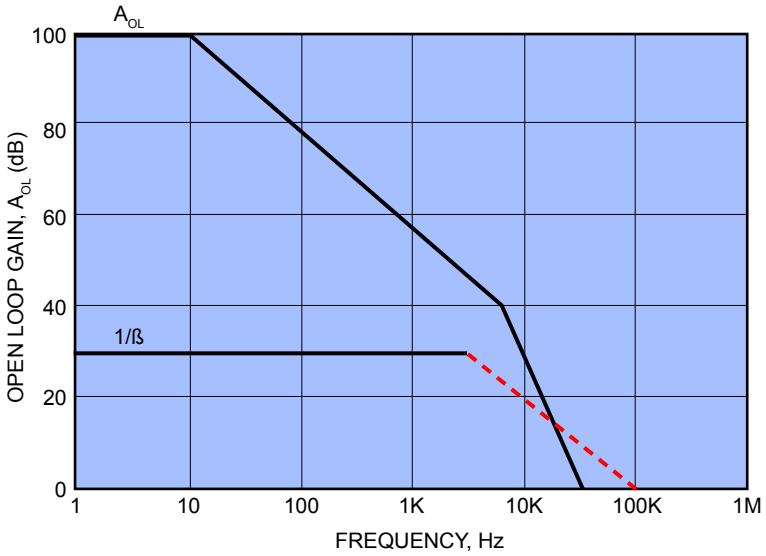


Figure 7. Feedback Zero Compensation

3.2 NOISE GAIN COMPENSATION

Figure 8 illustrates how noise gain compensation functions. This technique adds a parallel Z_I path through R_I and C_I, as shown in Figure 8. The objective with this technique is to close the loop gain early.

One way to view noise gain circuits is to view the amplifier as a summing amplifier. Consequently, there are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed via ground through the series combination of R_I and C_I. Since this is a summing amplifier, V_{OUT}/V_{IN} will be unaffected if we sum zero via the R_I-C_I network. However, in the small signal AC domain, we will be changing the loop gain (1/ß) plot of the feedback. Consequently, as C_I becomes a short as the frequency rises, and if $R_I << R_{IN}$, the signal gain will be set by R_F/R_I. Notice in Figure 9 that when the capacitive reactance of C_I is large, the loop gain ($1/ß_1$) line is governed by R_{IN}. However, when the capacitive reactance of C_I becomes small, then R_I supplants R_{IN} as the input resistor accounting for the shift to the loop gain ($1/ß_2$) line crosses the open loop (A_{OL}) line at 20dB per decade.

The usable bandwidth is approximately 8kHz.

The noise gain technique is largely immune to component tolerance variations. However, it is only appropriate for non-inverting amplifiers, i.e., summing configurations, and it does sacrifice closed loop gain, and therefore loop bandwidth at higher frequencies.

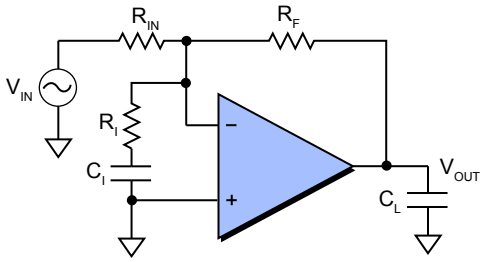


Figure 8. Noise Gain Compensation - Circuitry

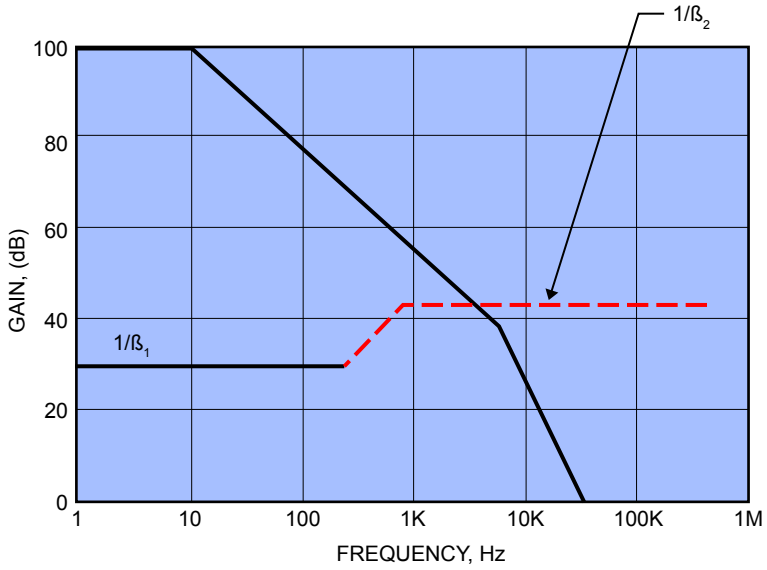


Figure 9. Noise Gain Compensation - Plots

3.3 ISOLATION RESISTOR COMPENSATION

Figure 10 illustrates isolation resistor compensation with resistor R_{ISO} connected in series with the load C_L. As depicted in Figure 11, the loop gain (1/ß) line, if uncompensated, would intersect the open loop gain (A_{OL}) line where the phase shift is 40dB per decade so that the circuit would be unstable. The resistor isolation compensation technique restores the 20dB per decade slope to the Bode Plot amplifier gain plot, as depicted by the red line in Figure 11, by inserting a resistor between the output of the amplifier and the capacitive load.

Note that resistor R_{ISO} adds a corner frequency or zero in the open loop (A_{OL}) plot, restoring a 20dB per decade slope before the 1/ß line intercepts it. The series impedance diminishes as the frequency rises so that at approximately 11kHz, the resistive load predominates as the series load. This technique does not sacrifice any loop gain because the open loop gain (A_{OL}) line remains stationary. However, the power loss in the resistor can be significant. The usable bandwidth is approximately 3kHz.

It is worth noting that there is virtually no loss in the peak voltage across the capacitive load because the current and voltage are out of phase. Consequently, when the peak voltage is maximum, the applied current is low, minimizing the voltage loss across the isolation resistor. This isolation resistor compensation technique is relatively immune to variations in component values.

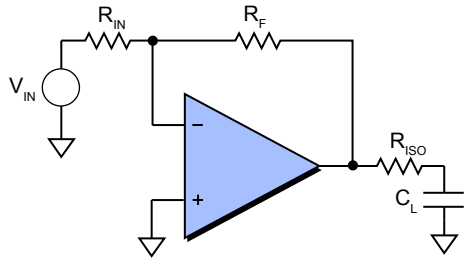


Figure 10. Isolation Resistor Circuitry

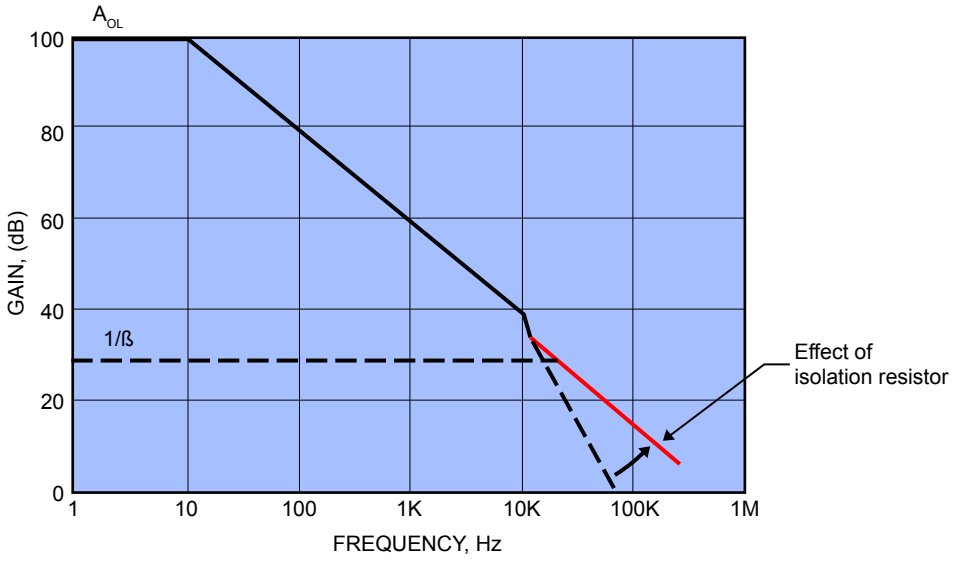


Figure 11. Isolation Resistor - Plot

4.0 STABILITY TESTS

The following tests describe test techniques for ascertaining whether a design will indeed perform in a stable way.

4.1 SQUARE WAVE TESTING

In this test, a small-amplitude square wave is injected into the closed loop op amp circuit as the V_{IN} source, as depicted in Figure 12. This example uses components as close to the production version as possible − including power supplies, cables and circuit boards.

A frequency should be chosen that is well within the loop gain bandwidth, but high enough to make triggering of an oscilloscope easy. For most applications, 1kHz is a good test frequency. Since we are interested in the small signal AC behavior, adjust V_{IN} so that the output is 200mV_{P-P} or less. This is to avoid large signal limitations such as slew rate, output current limitations and output voltage saturation. Check the 1kHz output (V_{OUT}) for overshoot and undershoot while exercising the circuitry, including the power supply with low-frequency variations.

Phase margin for a given step response can be estimated from Figure 13.

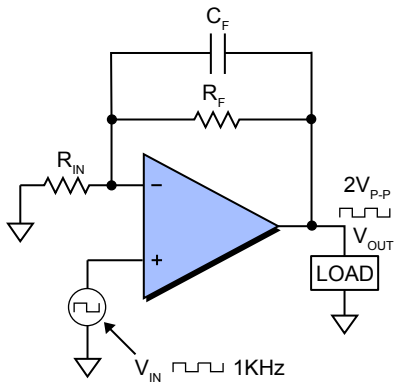


Figure 12. Square Wave Testing

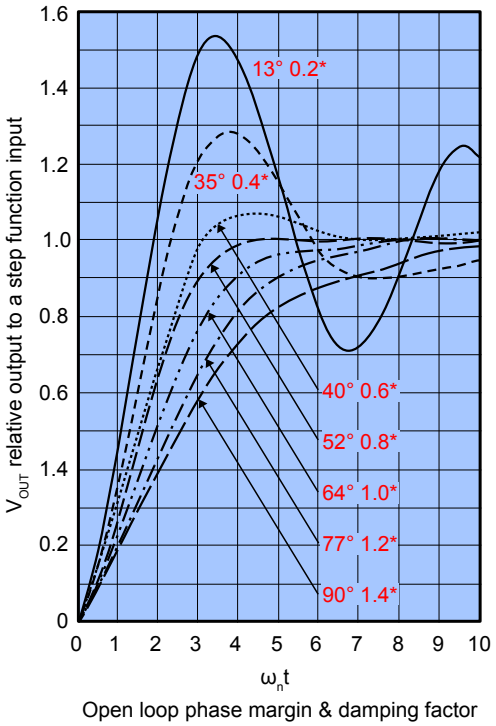


Figure 13. Phase Margin Versus Step Response

4.2 DYNAMIC STABILITY TEST

This is an expansion of the square wave test described in Section 4.1. The dynamic stability test is depicted in Figure 14. In this test a small-signal AC square wave is imposed on a low-frequency, large signal AC sine wave to dynamically test the power op amplifier under all operating point conditions. The square wave impressed on the slow moving 10-Hz sweep is depicted in Figure 15. Note that the value of R_1 in parallel with R_2 in Figure 14 must be much greater than R_I. Otherwise, the input test impedances will adversely affect the compensation of the op amp undergoing test.

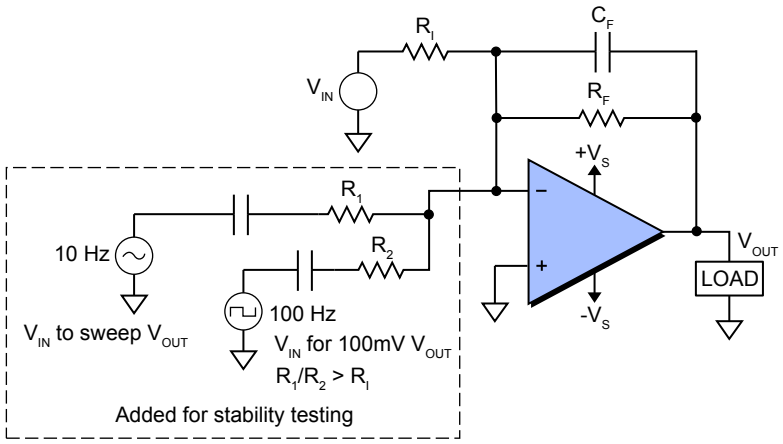


Figure 14. Dynamic Stability Test

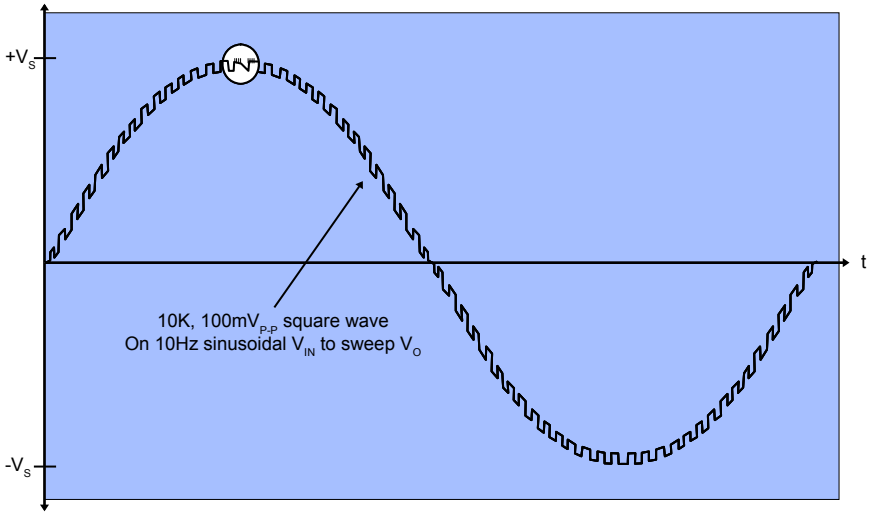


Figure 15. Square Wave Imposed on the Waveform

5.0 EXAMPLES

Shown in Figure 16 is an uncompensated op amp. Its Bode Plot is depicted in Figure 17. In the following sections we shall show how this circuit can be stabilized using the various stabilization techniques initially described in Section 3.

Note that the 50k pole in the open loop gain (A_{OL}) is due to the capacitive load impedance. This circuit is unstable because the closed loop gain 1/ß intersects the open loop gain at a rate of 40dB per decade.

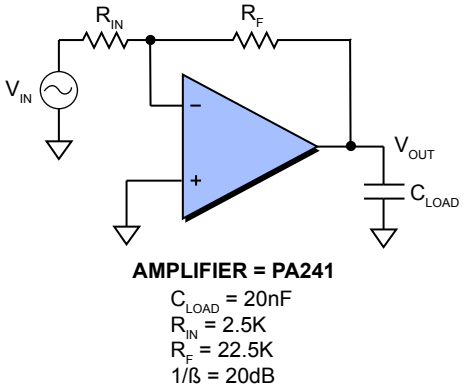


Figure 16. Uncompensated Op Amp

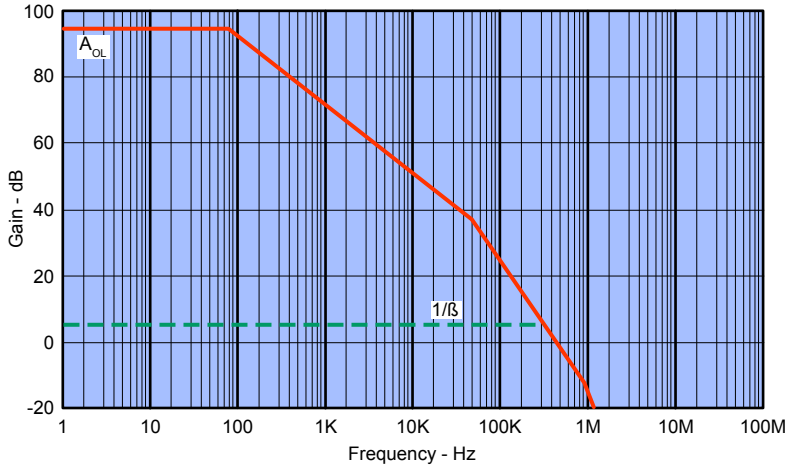


Figure 17. Uncompensated Op Amp − Bode Plot

5.1 FEEDBACK ZERO COMPENSATION

By adding a compensating capacitor C_F, to the circuit shown in Figure 16, the circuit becomes the one shown in Figure 18, and its corresponding bode response in Figure 19. By adding a feedback capacitor C_F to alter the 1/ß line, and placing a pole in the 1/ß plot so that it intersects the red line at an angle corresponding to less than 40db per decade, which happens to be just under 200kHz, the usable bandwidth is approximately 30KHz. This technique is very sensitive to the tolerances of the feedback capacitor. Note in the plot that the 20% capacitor moves that pole over a 100kHz range, so it is very susceptible to going in and out of stability based on that capacitor (which may change in value with changes in temperature).

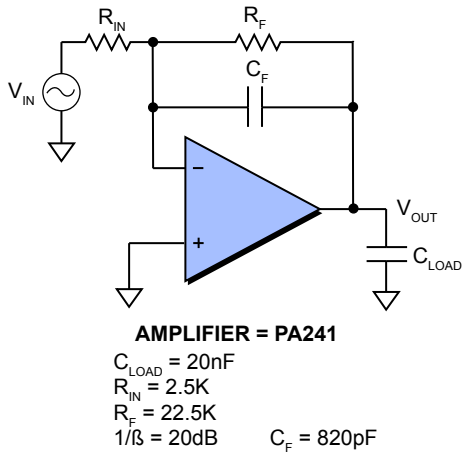


Figure 18. Compensated Capacitive Load – Schematic

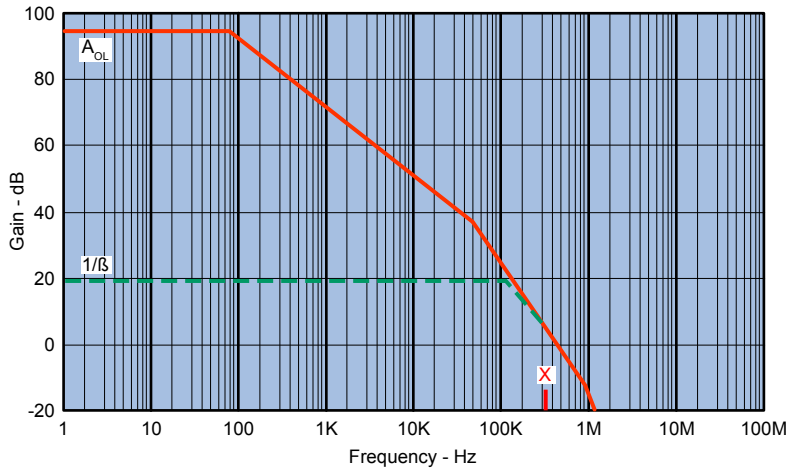


Figure 19. Compensated Capacitive Load – Bode Plot

5.2 CAPACITIVE LOAD – NOISE GAIN COMPENSATED

Shown in Figures 20 and 21 is a circuit and its corresponding Bode amplitude plot for an op amp employing noise gain compensation. The impact of adding C_N is to bump up the 1/ß (the green line) so that it intersects the A_{OL} line above the pole where the plot shifts from 20dB per decade (stable) to 40dB per decade (unstable).

The usable bandwidth is approximately 3kHz.

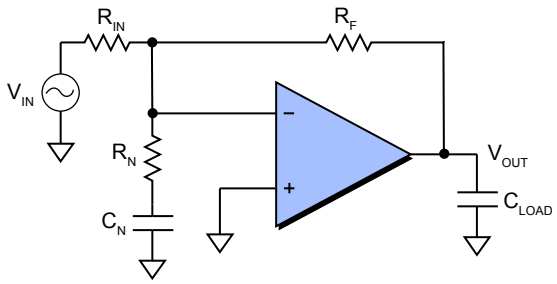


Figure 20. Noise Gain Compensated – Schematic

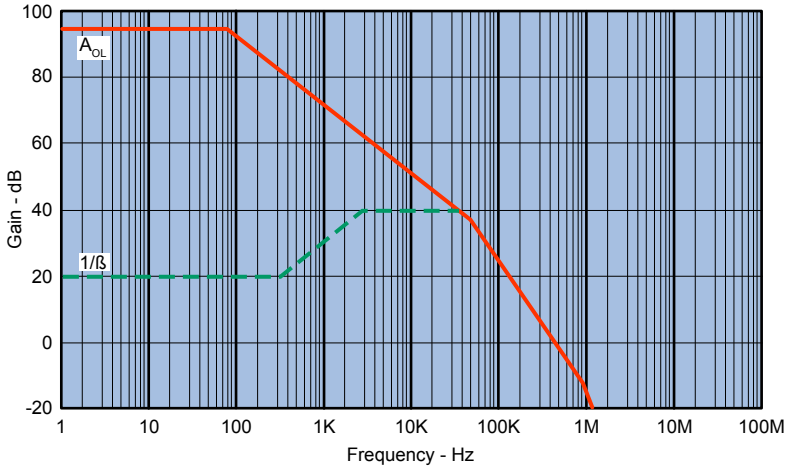
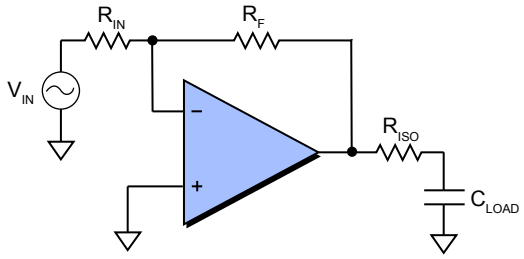


Figure 21. Noise Gain Compensated – Bode Plot

5.3 CAPACITIVE LOAD – ISOLATION RESISTOR

Shown in Figures 22 and 23 is a circuit and its corresponding Bode amplitude plot for an op amp employing an isolation resistor R_{ISO}. The isolation resistor reduces the phase angle of the load so that it doesn't appear capacitive at higher frequencies. The usable bandwidth is approximately 30kHz.

With the isolation resistor, we sacrifice virtually no bandwidth. This can be a significant trade off. In this case, with an 80 V_{P-P} output at 25kHz, we are dissipating 0.75 watts in the resistor. Because the loss is load current related, it may or may not be a problem.



AMPLIFIER = PA241

C_{LOAD} = 20nF
R_{IN} = 2.5K
R_F = 22.5K
1/ß = 20dB R_{ISO} = 100Ω

Figure 22. Isolation Resistor Compensated – Schematic

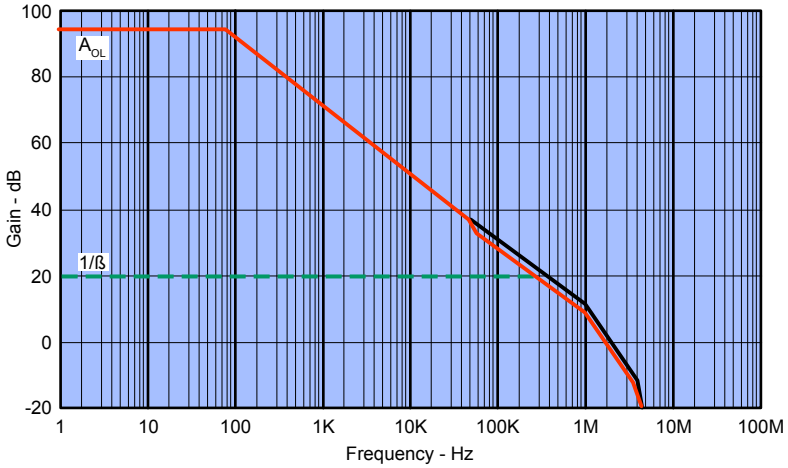


Figure 23. Isolation Resistor Compensated – Bode Plot

5.4 FEEDBACK ZERO AND NOISE GAIN COMPENSATED

Shown in Figures 24 and 25 is a circuit and its corresponding Bode amplitude plot for an op amp employing both feedback zero and noise gain compensation. The goal here is to use multiple techniques to lessen the impact of the trade offs. So with noise gain compensation bandwidth sacrificed, but with feedback zero compensation, circuit is quite sensitive to noise; however, with this combination we realize a usable bandwidth. It is back up in the neighborhood of 30kHz. The circuit is pretty much immune to component tolerance issues and finally there is good bit of phase margin.

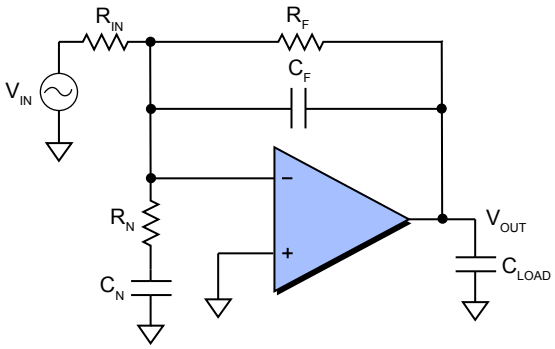


Figure 24. Capacitive & Noise Gain compensated – Schematic

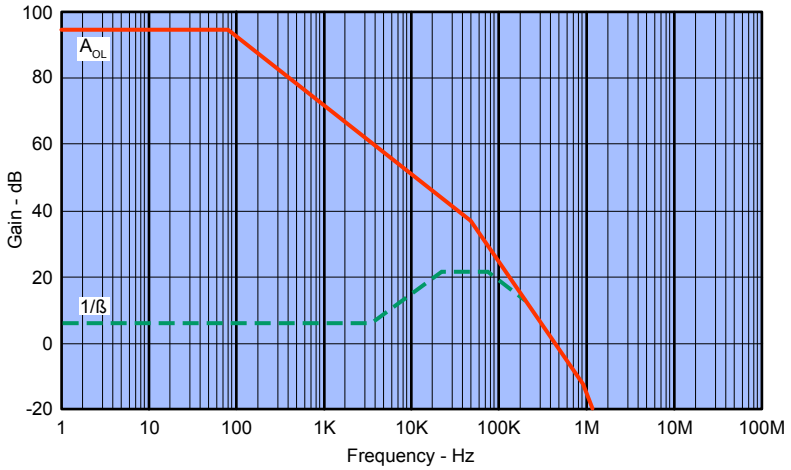


Figure 25. Capacitive & Noise Gain compensated – Bode Plot

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2. Apex Precision Power Application Note 19, *Stability For Power Operational Amplifiers*, Cirrus Logic, www.cirrus.com

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Intuitive Operational Amplifiers, Thomas M. Fredericksen, McGraw-Hill Book Co., 1988

REVISION HISTORY

Release	Date	Changes
REVA	APR 2008	Initial Release

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